

1910

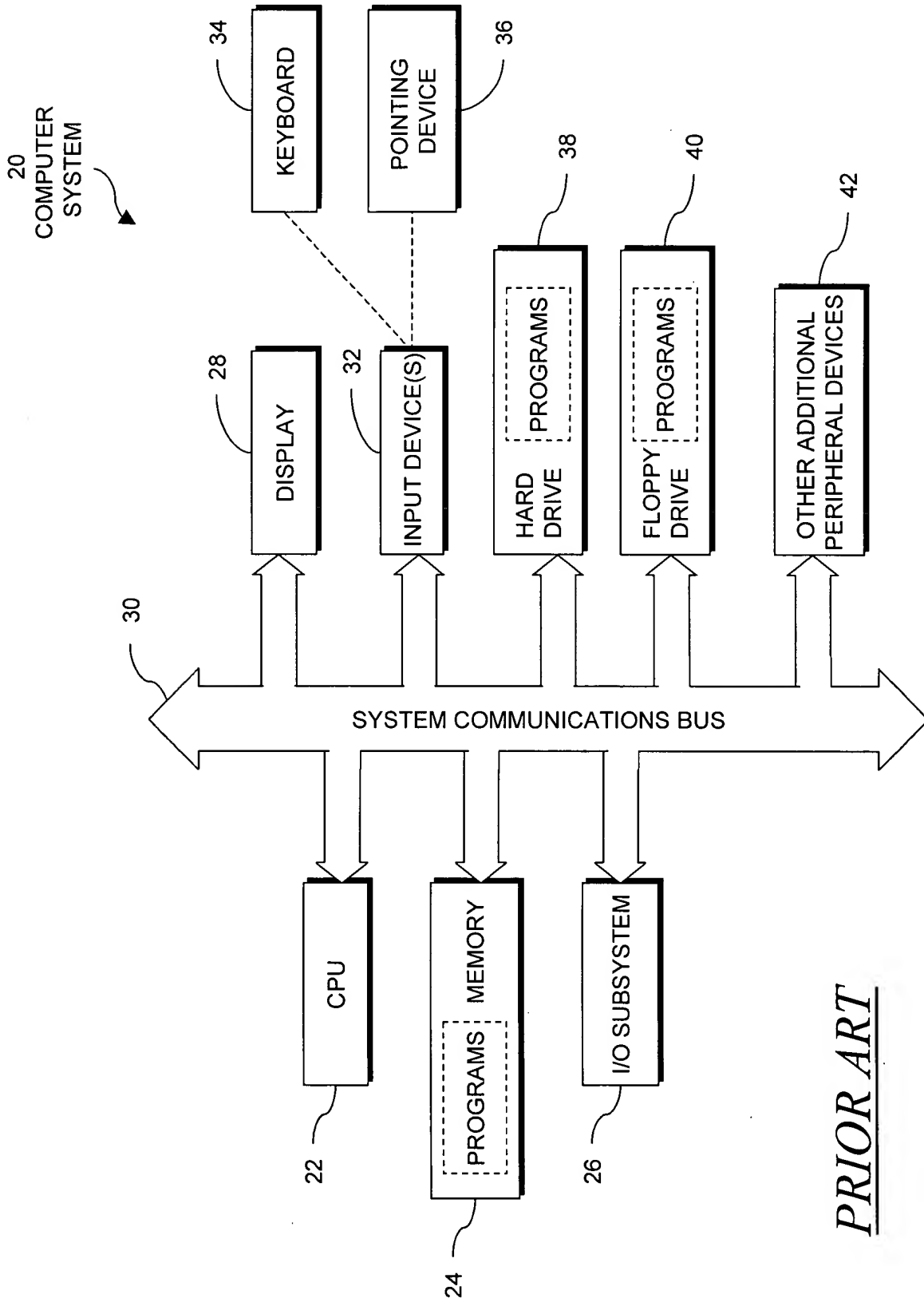


FIG. 1

PRIOR ART

2810

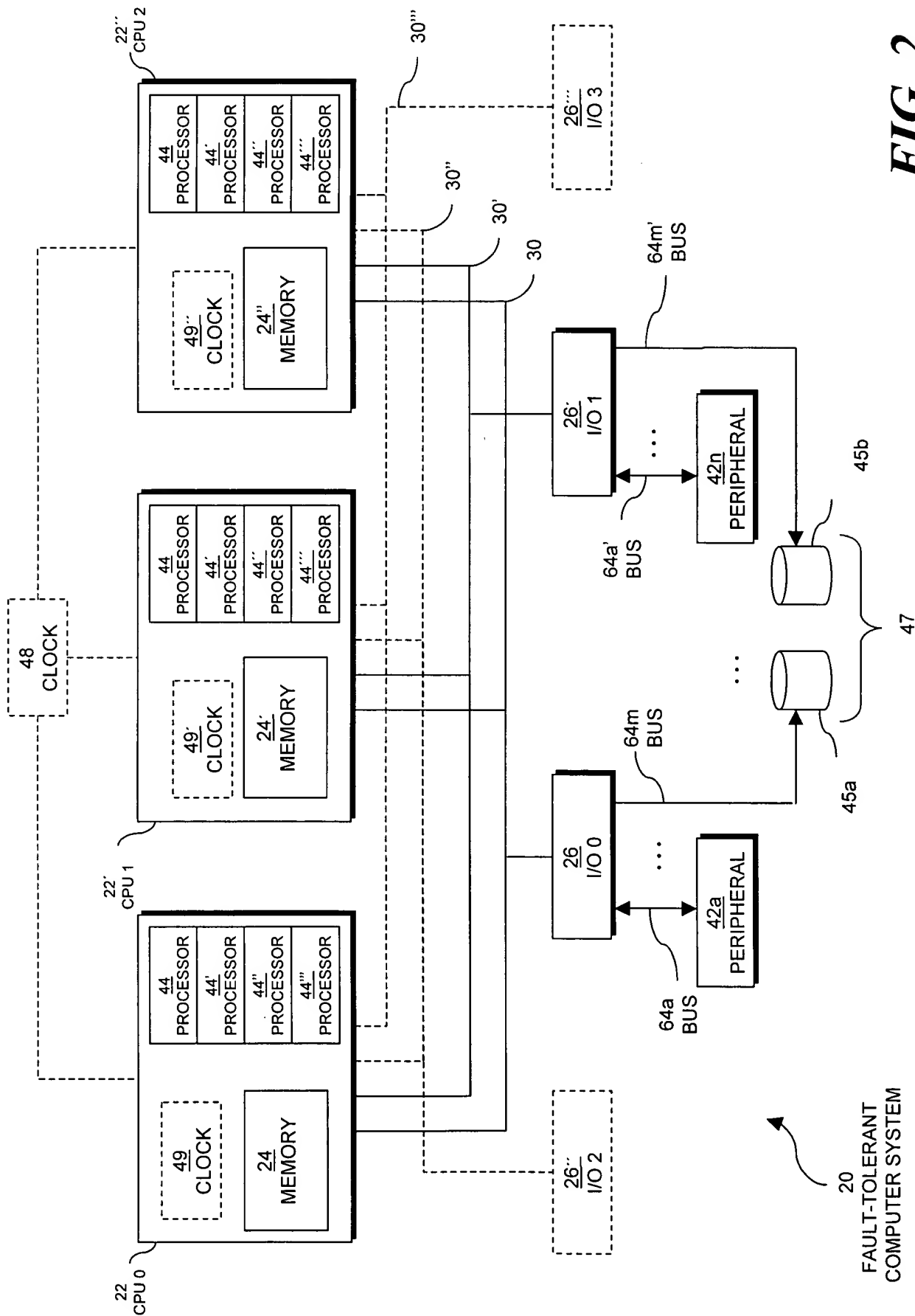


FIG. 2

FIG. 2 is a block diagram of a fault-tolerant computer system (20) according to one embodiment of the present invention. The system (20) includes three CPUs (22' CPU 0, 22'' CPU 1, 22''' CPU 2) and a common bus (30). Each CPU (22') contains a clock (49''), memory (24''), and four processors (44'). The system (20) also includes I/O blocks (26' I/O 0, 26'' I/O 1, 26''' I/O 2) connected to the bus (30), each with its own bus (64a, 64a', 64m) and peripherals (42a, 42n). Storage devices (45a, 45b) are also connected to the bus (30). A common clock (48) is connected to all CPUs (22').

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20 FAULT-TOLERANT COMPUTER SYSTEM

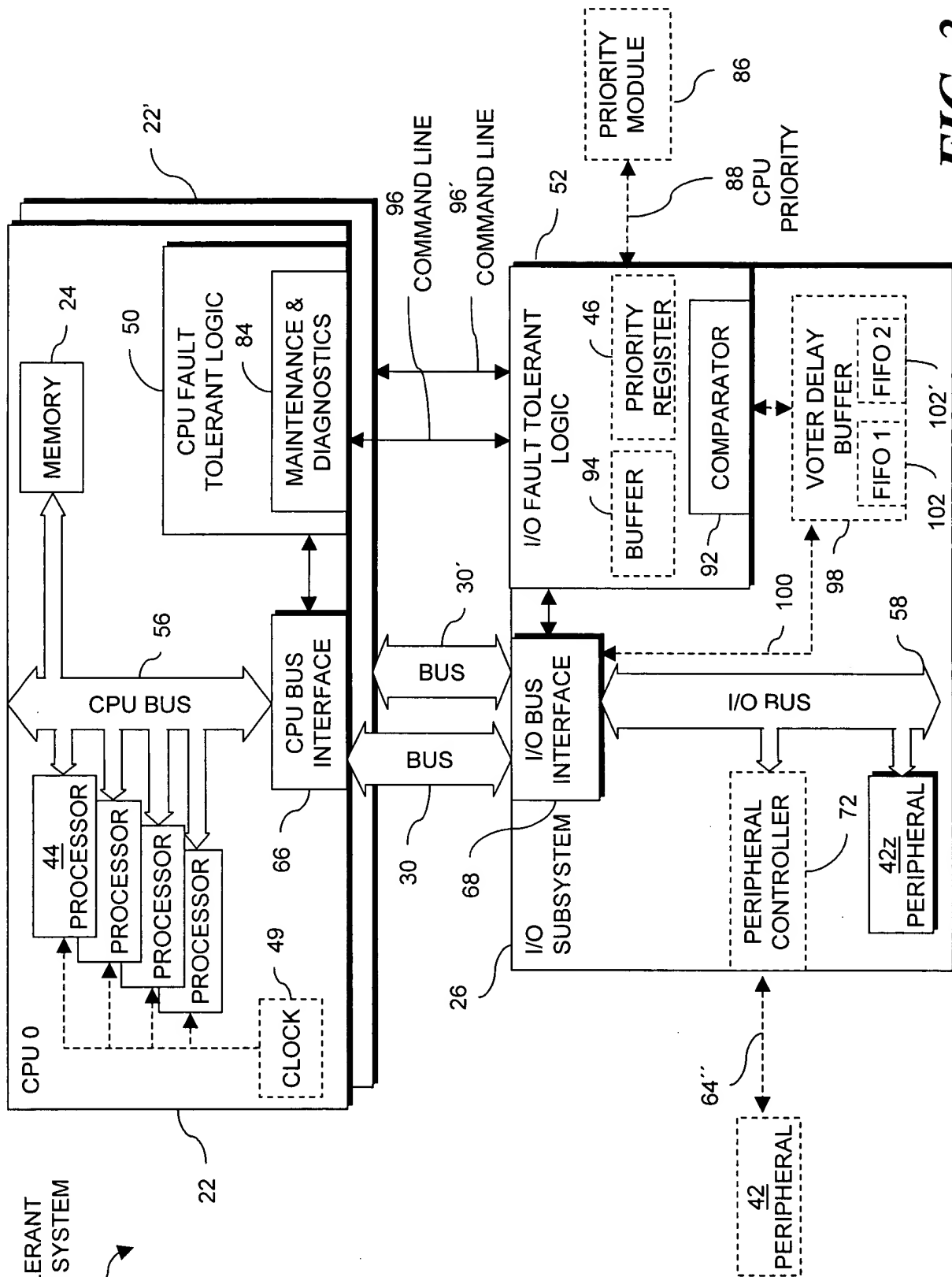


FIG. 3

4810

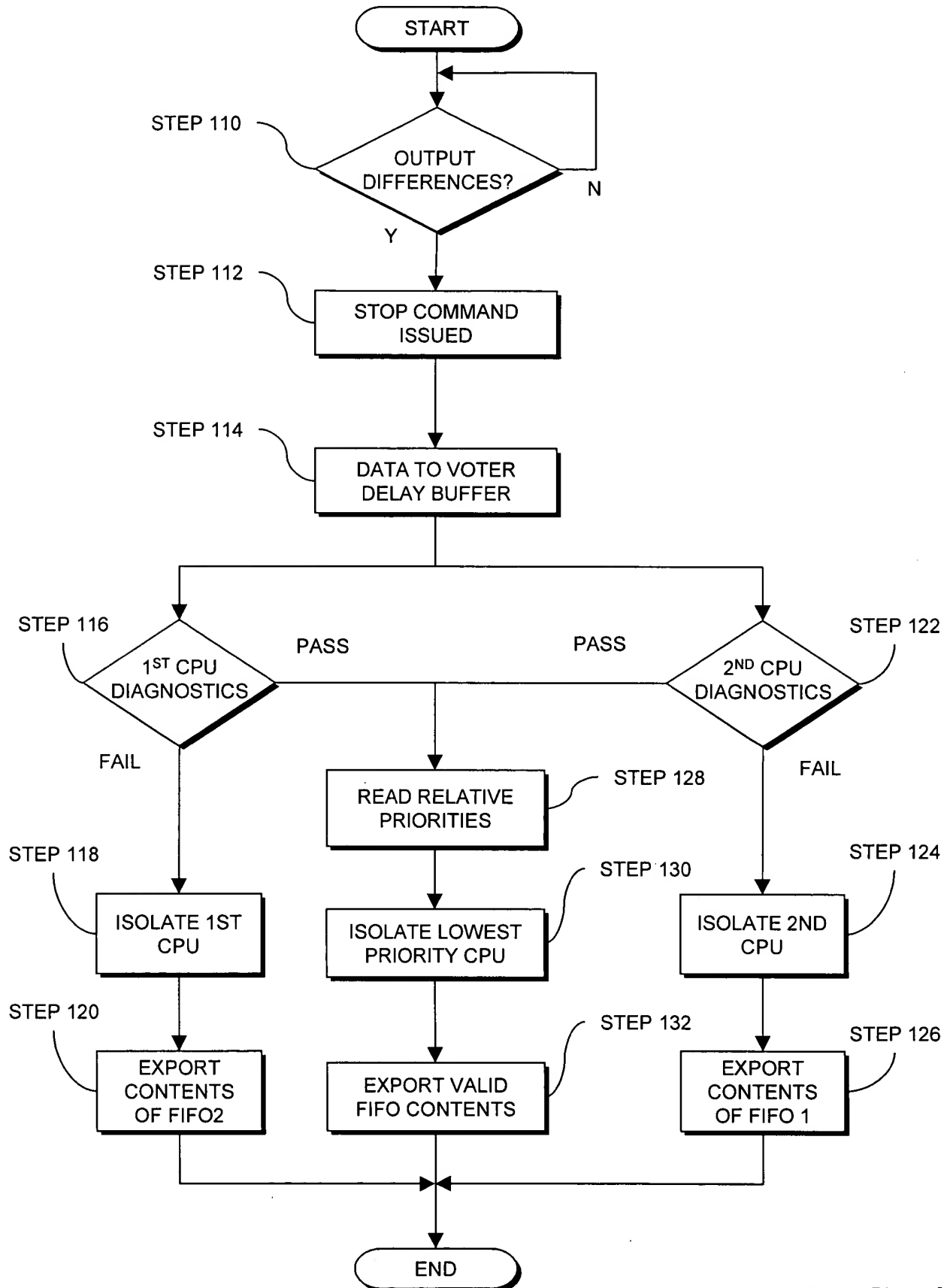


FIG. 4

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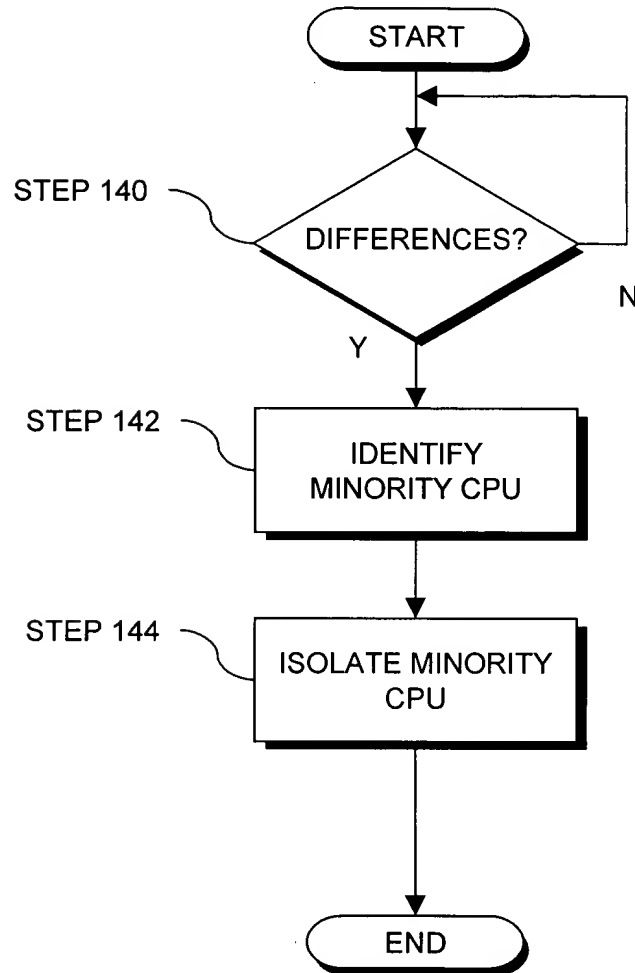


FIG. 5

6810

20
FAULT-TOLERANT
SERVER

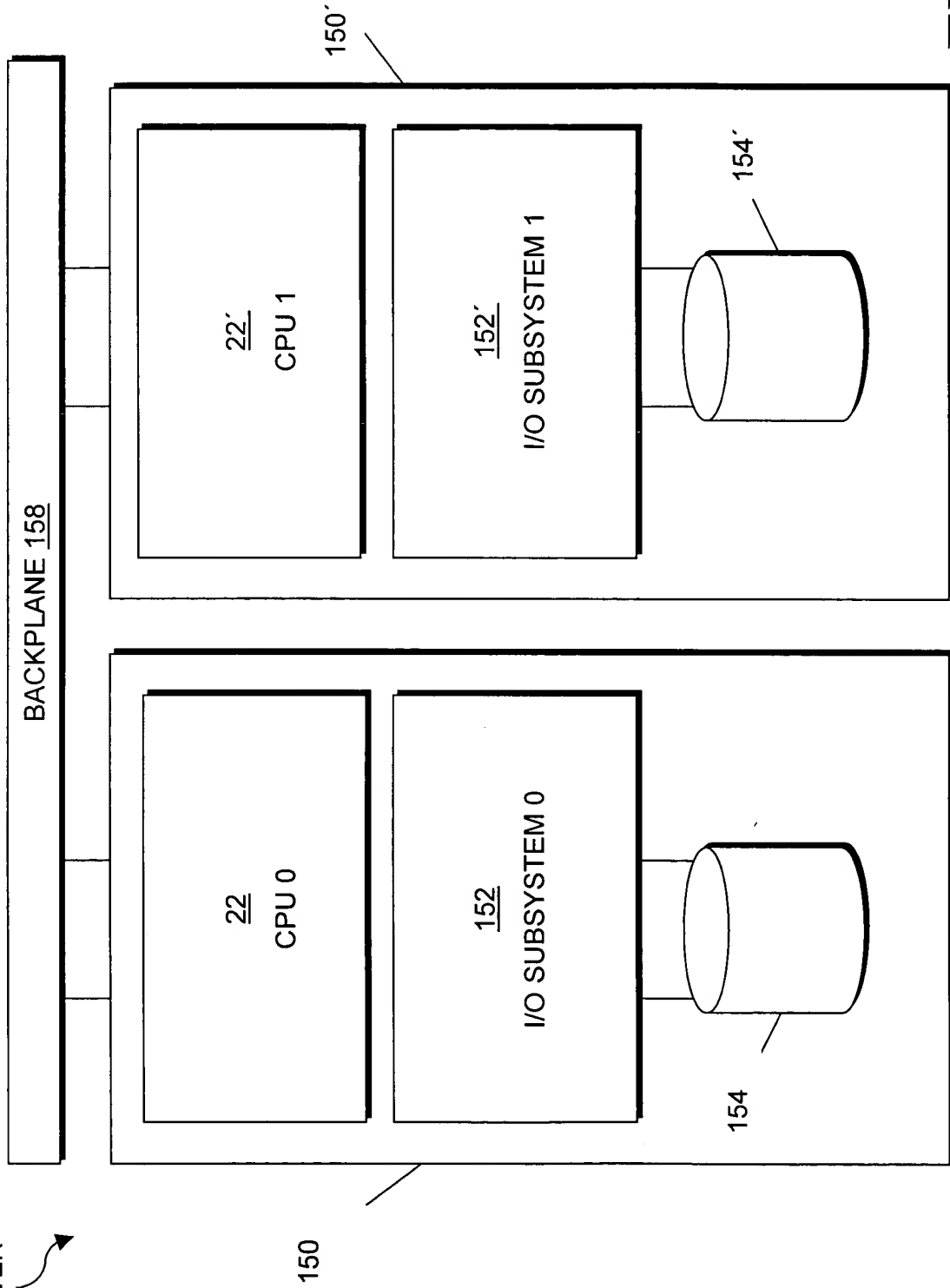


FIG. 6

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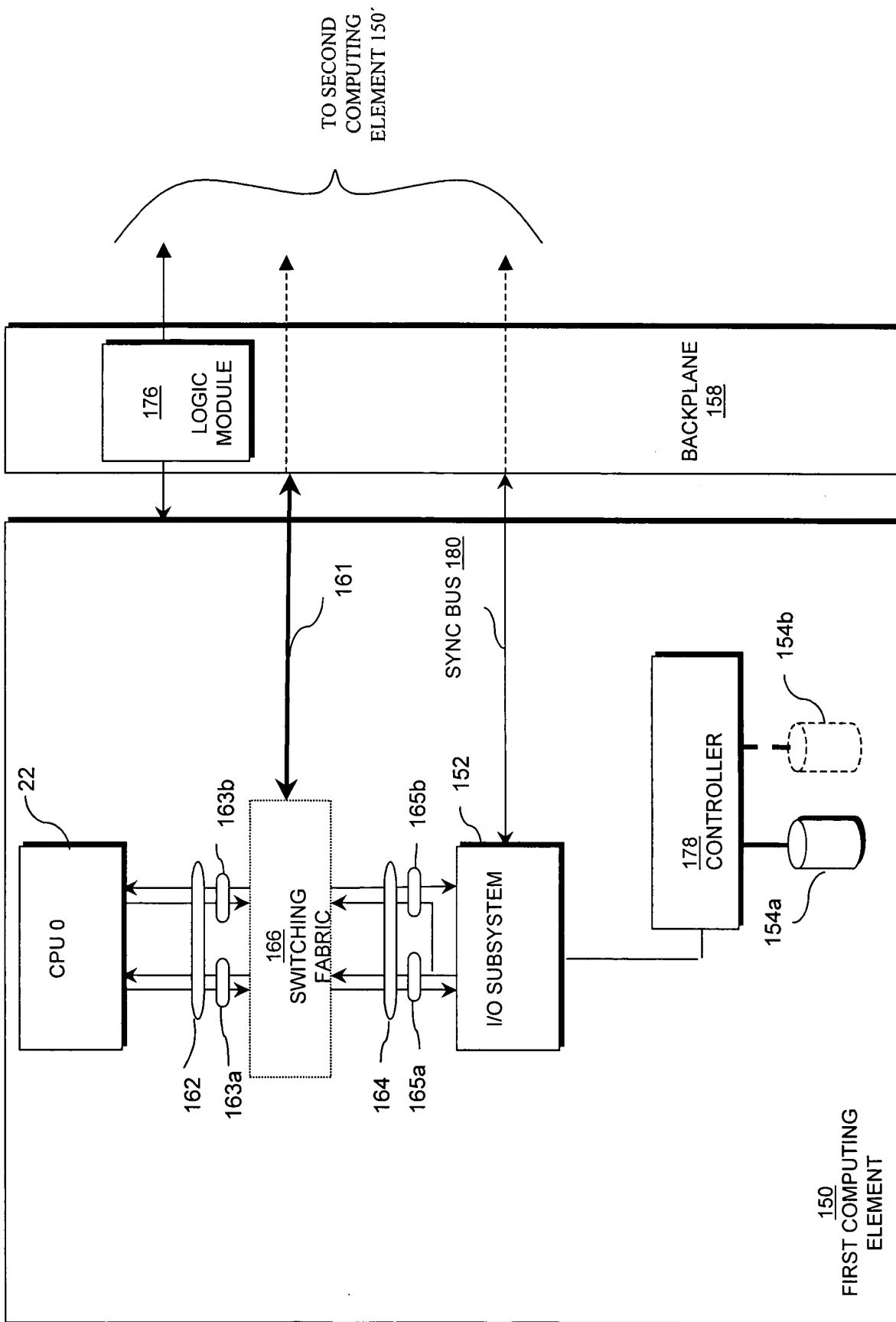


FIG. 7

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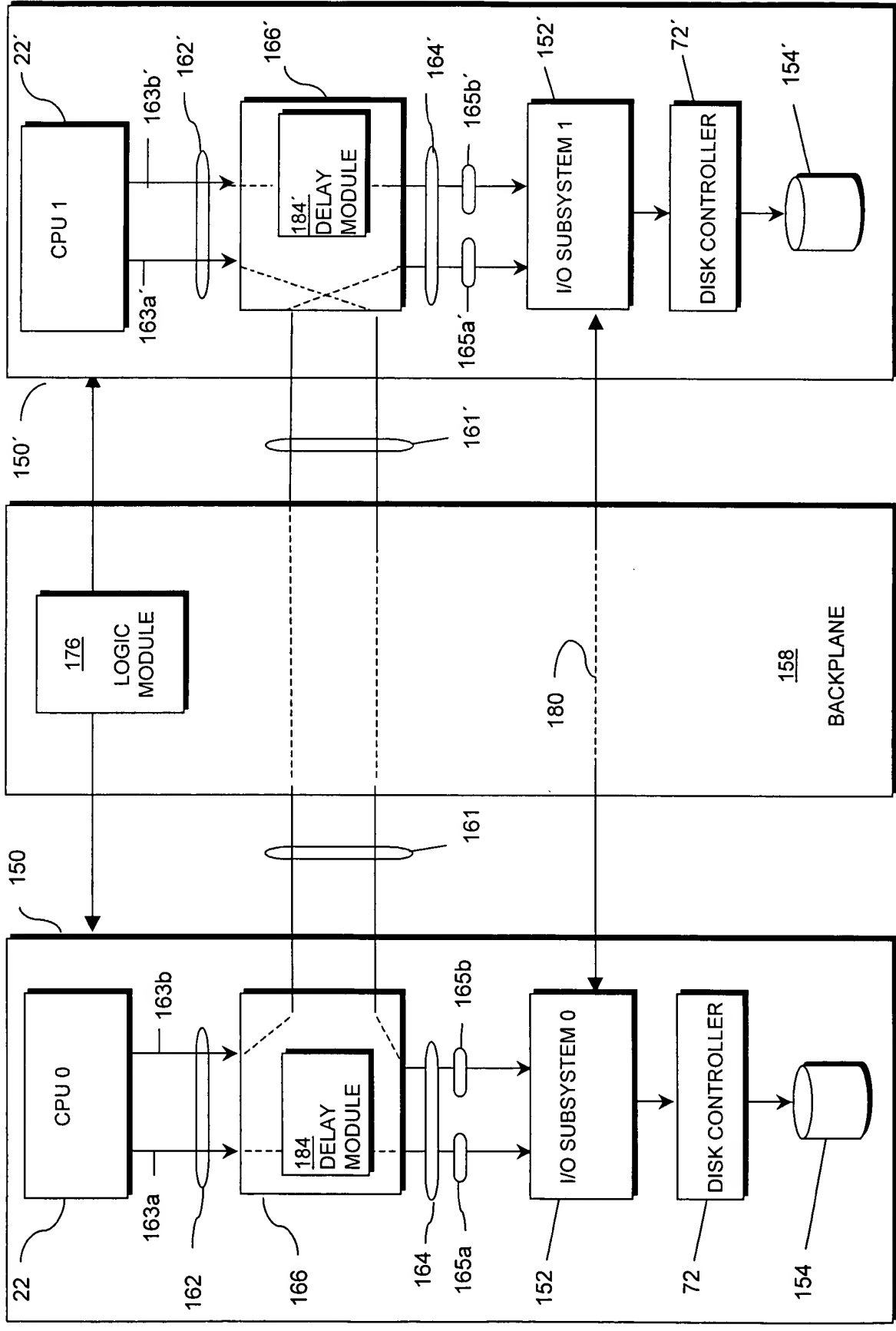


FIG. 8

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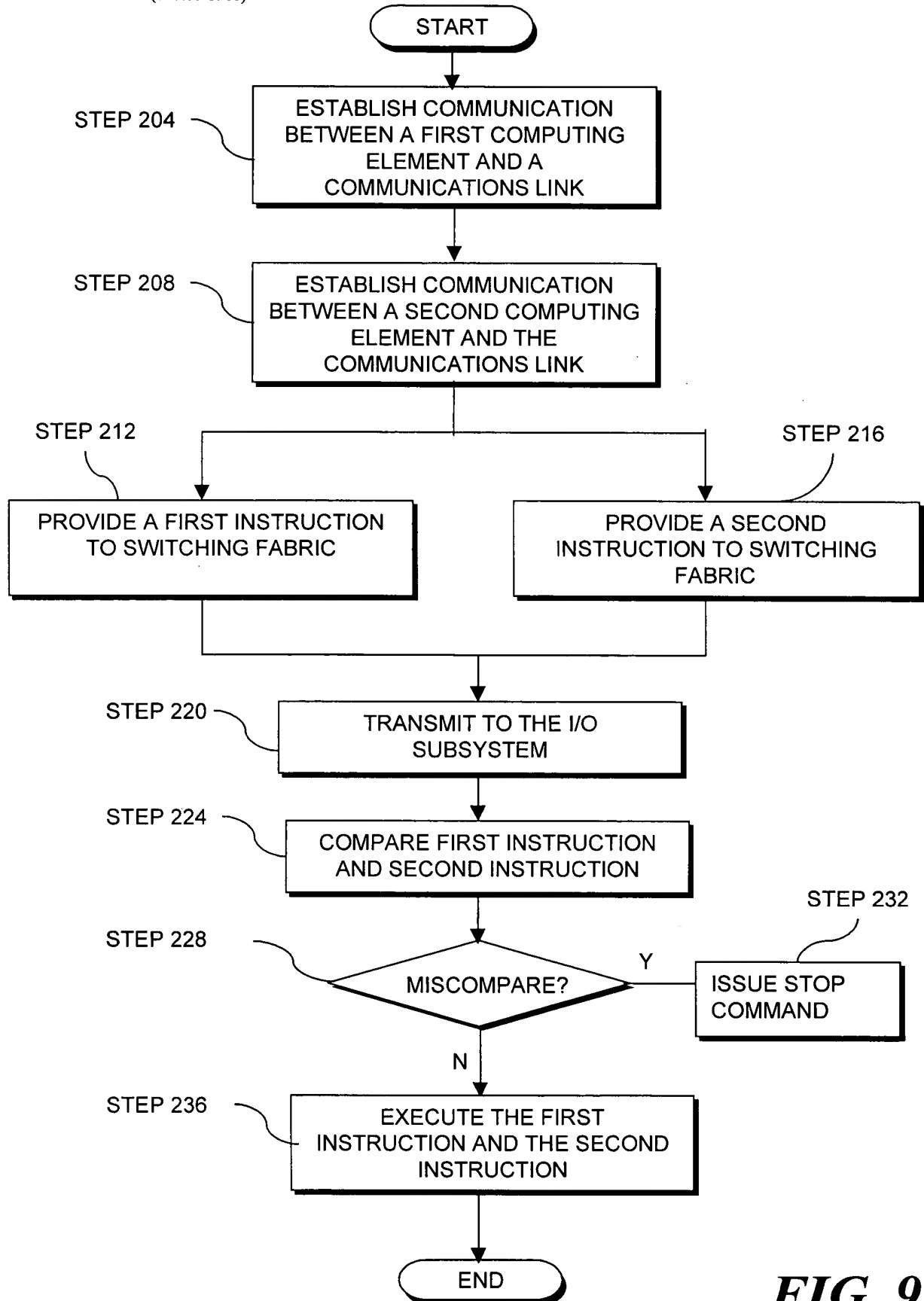


FIG. 9

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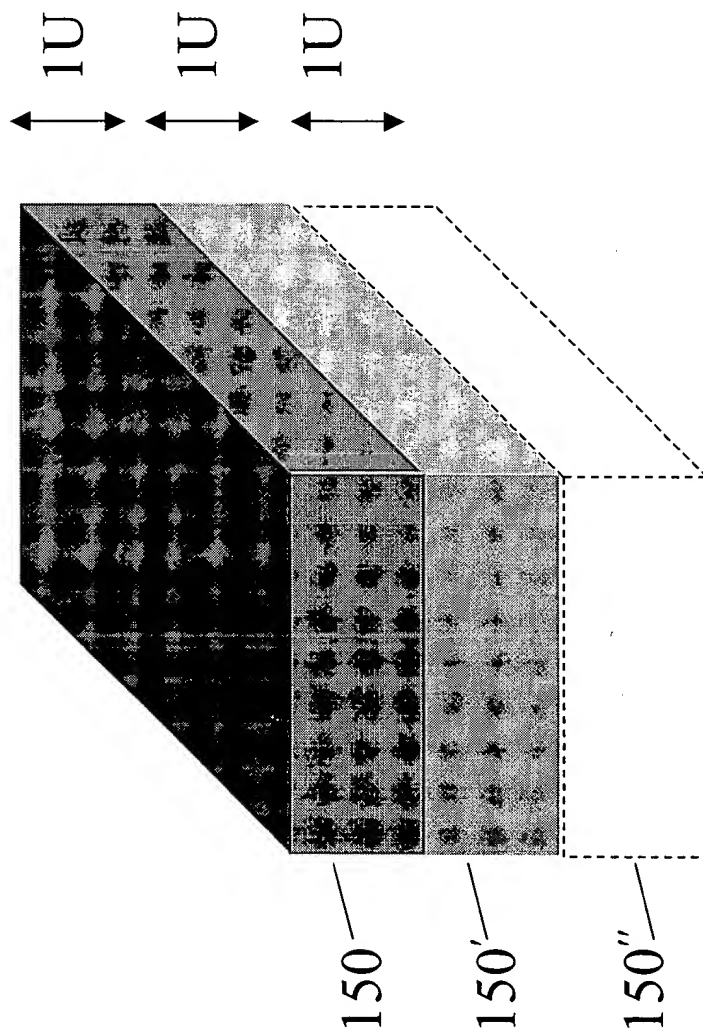


FIG. 10